



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Cheng, *et al.*

Docket No.: TSM03-0698

Filed: 2/25/2004

Examiner: Kevin Quinto

Serial No.: 10/786,643

Art Unit: 2826

Title: CMOS Structure and Related Method

Mail Stop Amendment  
Commissioner for Patents  
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Respectfully submitted,

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Serial No.: 10/786,643 Art Unit: 2826  
Filed: 02/25/2004 Examiner: Quinto, Kevin  
For: CMOS Structure and Related Method

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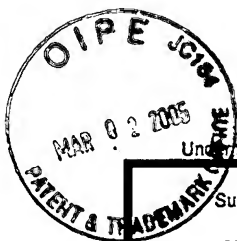
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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number	10/786,643
Filing Date	2/25/2004
First Named Inventor	Cheng, et al.
Art Unit	2826
Examiner Name	Quinto, Kevin
Attorney Docket Number	TSM03-0698

Sheet	1	of	6
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### U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code <sup>2</sup> (if known)			
	1	US-4,069,094	01-17-1978	Shaw et al.	
	2	US-4,314,269	02-02-1982	Fujiki	
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	38	US-6,429,061 B1	08-06-2002	Rim	
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				Art Unit	2826
Examiner Name	Quinto, Kevin				
Attorney Docket Number	TSM03-0698				
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		Country Code <sup>3</sup> - Number <sup>4</sup> - Kind Code <sup>5</sup> (if known)					
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	78	WO 03/017336 A2		02-27-2003	Amberwave Systems Corporation		

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Sheet	5	of	6	<i>Attorney Docket Number</i>	TSM03-0698

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	94	LEITZ, C.W., et al., "Hole Mobility Enhancements In Strained Si/Si <sub>1-y</sub> Ge <sub>y</sub> P-Type Metal-Oxide-Semiconductor Field-Effect Transistors Grown On Relaxed Si <sub>1-x</sub> Ge <sub>x</sub> (x<y) Virtual Substrates," Applied Physics Letters, Vol. 79, No. 25, December 17, 2001, pp. 4246-4248.	
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				Application Number	10/786,643
				Filing Date	2/25/2004
				First Named Inventor	Cheng, et al.
				Art Unit	2826
				Examiner Name	Quinto, Kevin
Sheet	6	of	6	Attorney Docket Number	TSM03-0698

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	105	SHAHIDI, G.G., "SOI Technology for the GHz Era," IBM J. Res. & Dev., Vol. 46, No. 2/3, March/May 2002, pp. 121-131.	
	106	SHIMIZU, A., et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement," IEDM 2001, pp. 433-436.	
	107	TEZUKA, T., et al., "High-Performance Strained Si-on-Insulator MOSFETs by Novel Fabrication Processes Utilizing Ge-Condensation Technique," Symposium On VLSI Technology Digest of Technical Papers, 2002, pp. 96-97.	
	108	THOMPSON, S., et al., "A 90 nm Logic Technology Featuring 50nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1 um <sup>2</sup> SRAM Cell," IEDM, December 2002, pp. 61-64.	
	109	TIWARI, S., et al., "Hole Mobility Improvement in Silicon-on-Insulator and Bulk Silicon Transistors Using Local Strain," International Electron Device Meeting, 1997, pp. 939-941.	
	110	WANG, L.K., et al., "On-Chip Decoupling Capacitor Design to Reduce Switching-Noise-Induced Instability in CMOS/SOI VLSI," Proceedings of the 1995 IEEE International SOI Conference, Oct. 1995, pp. 100-101.	
	111	WELSER, J., et al., "NMOS and PMOS Transistors Fabricated in Strained Silicon/Relaxed Silicon-Germanium Structures," IEDM, 1992, pp. 1000-1002.	
	112	WONG, H.-S.P., "Beyond the Conventional Transistor," IBM J. Res. & Dev., Vol. 46, No. 2/3, March/May 2002, pp. 133-167.	
	113	YANG, F.L., et al., "35nm CMOS FinFETs," Symposium on VLSI Technology Digest of Technical Papers, 2002, pp. 104-105.	
	114	YANG, F.L., et al., "25 nm CMOS Omega FETs," IEDM, 2002, pp. 255-258.	
	115	YEOH, J.C., et al., "MOS Gated Si:SiGe Quantum Wells Formed by Anodic Oxidation," Semicond. Sci. Technol., Vol. 13, 1998, pp. 1442-1445.	

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